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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/866,662	05/30/2001	Hideaki Kuroda	SON-1199/CON	6271

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EXAMINER	
PRENTY, MARK V	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/866,662	KURODA, HIDEAKI	
	Examiner	Art Unit	
	MARK V PRENTY	2822	

-- The MAILING DATE of this communication appears on the cover sh et with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3 and 4* is/are rejected.

7)☒ Claim(s) *5 and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This non-final Office Action is in response to the response filed on March 10, 2004.

Claims 3 and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Jost et al. (newly cited United States Patent 5,605,857 – hereafter Jost).

With respect to independent claim 3, Jost discloses a semiconductor device (see the entire patent, including Fig. 1 and Fig. 5), comprising: a conductive layer pattern 22/24/26 formed on a substrate 11; a first inter-layer insulating film 18/20/28 which covers said conductive layer pattern and is formed on said substrate; a first connection hole formed in an upper layer 28 of said first inter-layer insulating film above said conductive layer pattern; a second connection hole which reaches said conductive layer pattern 24 from the bottom portion of said first connection hole and then has a smaller diameter than that of said first connection hole and formed on said first inter-layer insulation film; a plug 45 having conductivity and filling internal portions of said first connection hole and said second connection hole; a second inter-layer insulating film 46 formed on said first inter-layer insulating film, wherein said second inter-layer insulating film includes up to five layers; a third connection hole which reaches said plug and is formed through said second inter-layer insulating film; and a conductive portion 55 which is connected to said plug and formed in said third connection hole.

Claim 3 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Jost.

With respect to independent claim 4, Jost discloses a semiconductor device (see the entire patent, including Fig. 1 and Fig. 5), comprising: a conductive layer pattern

22/24/26 formed on a substrate 11; a first inter-layer insulating film 18/20/28 which covers said conductive layer pattern and is formed on said substrate; a first connection hole formed in an upper layer 28 of said first inter-layer insulating film above said conductive layer pattern; a second connection hole which reaches said conductive layer pattern 24 from the bottom portion of said first connection hole and then has a smaller diameter than that of said first connection hole and formed on said first inter-layer insulation film; a plug 45 having conductivity and filling internal portions of said first connection hole and said second connection hole, wherein the upper surface of said plug is formed to almost the same height as the surface height of said first inter-layer insulating film; a second inter-layer insulating film 46 formed on said first inter-layer insulating film, wherein said second inter-layer insulating film includes up to five layers; a third connection hole which reaches said plug and is formed through said second inter-layer insulating film; and a conductive contact portion 55 which is connected to said plug and formed in said third connection hole.

Claim 4 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Jost.

Claims 5 and 6 are objected to as being dependent upon a rejected base claim, but would be allowable over the prior art of record if rewritten in independent form including all of the limitations of the base claim and any intervening claims (although it would be more accurate to say that the plug and conductive portion form a storage node contact portion and a storage node, respectively, of a dynamic random access memory – see the specification at the paragraph bridging pages 20-21).

The prior art does not disclose or suggest the allowable semiconductor devices taken as a whole, including the plug and conductive portion being a storage node contact portion (and a storage node, respectively) of a dynamic random access memory.

The applicant's arguments with respect to the previous rejection of claims 3-6 under 35 U.S.C. 102 as being anticipated by Prior Art Fig. 3 are not persuasive, but that rejection is nevertheless hereby withdrawn. Specifically, Prior Art Figs. 3 and 17 are different (but intersecting) cross-sections of the same semiconductor device (illustrated in plan view in Prior Art Fig. 2). The Prior Art Fig. 3 cross-section shows a portion of the device where the second inter-layer insulating film ostensibly includes only five layers (culminating in layer 164). The Prior Art Fig. 17 cross-section shows a portion of the device where the second inter-layer insulating film ostensibly varies from having six layers (see Prior Art Fig. 17's left edge) to having five layers (see Prior Art Fig. 17 at the area between conductive portions 144, which is the point of intersection with Prior Art Fig. 3). The reason Prior Art Figs. 2-17's second inter-layer insulating film ostensibly varies from having six layers to having only five layers is that insulating layer 163 is shaved off in the area of the bit line BL (see the Prior Art Figs. 12-13 disclosure). The previous rejection of claims 3-6 is thus withdrawn if only because Prior Art Figs. 2-17's second inter-layer insulating film as a whole includes six layers.

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.

Mark Prenty

Mark V. Prenty
Primary Examiner